

WHAT IS CLAIMED IS:

1. A semiconductor device which includes a semiconductor layer provided on a buried insulating film on a substrate, and device-isolation regions dividing the semiconductor layer into a plurality of active regions, and in which a first transistor having
5 a channel of a first conductivity type is provided in a first active region of the active regions, and a second transistor having a channel of a second conductivity type is provided in a second active region of the active regions,
wherein the first transistor includes:
a first source region of the first conductivity type, which is formed within the first
10 active region;
a first drain region of the first conductivity type, which is formed within the first active region so as to be spaced apart from the first source region;
a first body region of the second conductivity type, which is formed within the first active region so as to be located adjacent to the first source region;
15 a first gate insulating film, which is formed on the active region and has a thin film portion and a thick film portion, wherein the thin film portion is formed closer to the source by a gate oxidation process, and the thick film portion is formed closer to the drain by a LOCOS technique and connected to the thin film portion;
a first drain offset region of the first conductivity type, which is formed adjacent to
20 the first drain region within the first active region, and has an impurity-concentration peak in a deep portion located a certain depth-extent below the lower face of the thick film portion of the first gate insulating film; and
a gate electrode, which extends over the thin film portion and a part of the thick film portion of the first gate insulating film.

2. The device of Claim 1, wherein the deep portion of the first drain offset region is to an extent at which the on-resistance of the first transistor is equal to or less than a first established value.

5 3. The device of Claim 1, wherein the deep portion of the first drain offset region is an extent of 10% through 60% into the thickness of the semiconductor layer beneath the thick film portion in depth from the lower face of the thick film portion.

4. The device of Claim 1, wherein the deep portion of the first drain offset region is
10 an extent of 20% through 40% into the thickness of the semiconductor layer beneath the thick film portion in depth from the lower face of the thick film portion.

5. The device of Claim 1, wherein the deep portion of the first drain offset region is to an extent at which the source-to-drain breakdown voltage of the first transistor is equal to
15 or greater than a second established value.

6. The device of Claim 1, wherein the deep portion of the first drain offset region is an extent of 25% through 60% into the thickness of the semiconductor layer beneath the thick film portion in depth from the lower face of the thick film portion.

20

7. The device of Claim 1, wherein the second transistor includes:
a second source region of the second conductivity type, which is formed within the second active region;

a second drain region of the second conductivity type, which is formed within the
25 second active region so as to be spaced apart from the second source region;

a second gate insulting film, which is formed by a LOCOS technique on a region of the active region which is located between the second source region and the second drain region;

5 a second body region of the first conductivity type, which is formed within the second active region so as to be located adjacent to the second source region, and has an impurity-concentration peak in a deep portion located a certain depth-extent below the lower face of the second gate insulating film;

a second drain offset region of the second conductivity type, which is formed adjacent to the second drain region within the second active region; and

10 a gate electrode, which is formed on the second gate insulating film.

8. The device of Claim 7, wherein the deep portion of the second body region is to an extent at which the source-to-drain breakdown voltage of the second transistor is equal to or greater than a third established value.

15

9. A semiconductor device which includes a semiconductor layer provided on a buried insulating film on a substrate, and device-isolation regions dividing the semiconductor layer into a plurality of active regions, and in which a first transistor having a channel of a first conductivity type is provided in a first active region of the active regions, and a second transistor having a channel of a second conductivity type is provided in a second active region of the active regions,

wherein the second transistor includes:

a second source region of the second conductivity type, which is formed within the second active region;

25 a second drain region of the second conductivity type, which is formed within the

second active region so as to be spaced apart from the second source region;

a second gate insulting film, which is formed by a LOCOS technique on a region of the active region which is located between the second source region and the second drain region;

5 a second body region of the first conductivity type, which is formed within the second active region so as to be located adjacent to the second source region, and has an impurity-concentration peak in a deep portion located a certain depth-extent below the lower face of the second gate insulating film;

a second drain offset region of the second conductivity type, which is formed
10 adjacent to the second drain region within the second active region; and

a gate electrode, which is formed on the second gate insulating film.

10. The device of Claim 9, wherein the deep portion of the second body region is to an extent at which the source-to-drain breakdown voltage of the second transistor is equal to
15 or greater than a third established value.

11. The device of Claim 9, wherein the deep portion of the second body region is an extent of 25% through 60% into the thickness of the semiconductor layer beneath the second gate insulating film in depth from the lower face of the second gate insulating film.

20

12. A method for fabricating a semiconductor device which includes a semiconductor layer provided on a buried insulating film on a substrate, and device-isolation regions dividing the semiconductor layer into a plurality of active regions, and in which a first transistor having a channel of a first conductivity type is provided in a first
25 active region of the active regions, and a second transistor having a channel of a second

conductivity type is provided in a second active region of the active regions, the method comprising the steps of:

(a) implanting ions of an impurity of the second conductivity type into a region of the first active region in which a first body region is to be formed;

5 (b) implanting ions of an impurity of the first conductivity type into a region of the first active region, which is spaced apart from the first body region and in which a first drain offset region is to be formed, at a higher energy than that of the step (a);

(c) forming the first body region and the first drain offset region by heat treatment in such a manner that the first body region has a second-conductivity-type-impurity
10 concentration peak in a surface region of the semiconductor layer, while the first drain offset region has a first-conductivity-type-impurity concentration peak in a deep portion located a certain depth-extent below the lower face of a thick film portion that is to be formed later;

(d) forming by a LOCOS technique the thick film portion of a first gate insulating
15 film, on a region of the first drain offset region which is other than the both end portions of the first drain offset region, and is closer to the drain; and

(e) forming by a gate oxidation process a thin film portion of the first gate insulating film, which is connected to the thick film portion, on a region extending over from the first body region to the first-drain-offset-region end portion located closer to the
20 source.

13. The method of Claim 12, wherein the impurity-ion implantation in the step (b) is performed so that the deep portion of the first drain offset region is to an extent at which the on-resistance of the first transistor is equal to or less than a first established value, after the
25 step (d) has been completed.

14. The method of Claim 12, wherein the impurity-ion implantation in the step (b) is performed so that the deep portion of the first drain offset region is an extent of 10% through 60% into the thickness of the semiconductor layer beneath the thick film portion in depth
5 from the lower face of the thick film portion, after the step (d) has been completed.

15. The method of Claim 12, wherein the impurity-ion implantation in the step (b) is performed so that the deep portion of the first drain offset region is an extent of 20% through 40% into the thickness of the semiconductor layer beneath the thick film portion in depth
10 from the lower face of the thick film portion, after the step (d) has been completed.

16. The method of Claim 12, wherein the impurity-ion implantation in the step (b) is performed so that the deep portion of the first drain offset region is to an extent at which the source-to-drain breakdown voltage of the first transistor is equal to or greater than a second
15 established value, after the step (d) has been completed.

17. The method of Claim 12, wherein the impurity-ion implantation in the step (b) is performed so that the deep portion of the first drain offset region is an extent of 25% through 60% into the thickness of the semiconductor layer beneath the thick film portion in depth
20 from the lower face of the thick film portion, after the step (d) has been completed.

18. The method of Claim 12, wherein in the step (a) the ions of the impurity of the second conductivity type are also implanted into a region of the second active region in which a second drain offset region is to be formed;
25 in the step (b) the ions of the impurity of the first conductivity type are also

implanted into a region of the second active region, which is spaced apart from the second drain offset region and in which a second body region is to be formed; and

in the step (c) the second drain offset region and the second body region are formed in such a manner that the second drain offset region has a second-conductivity-type-impurity concentration peak in a surface region of the semiconductor layer, while the
5 second body region has a first-conductivity-type-impurity concentration peak in a portion located a certain depth-extent below the upper surface of the semiconductor layer.